IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Currently amended) A method of forming a semiconductor structure in a semiconductor wafer, the method comprising the steps of:

forming an epitaxial layer on a least a portion of a semiconductor substrate of a first conductivity type;

forming at least one trench in an upper surface of the semiconductor wafer and partially into the epitaxial layer;

forming at least one diffusion region between a bottom wall of the at least one trench and the substrate, the at least one diffusion region providing an electrical path between the bottom wall of the at least one trench and the substrate;

doping at least one or more sidewalls of the at least one trench with a first impurity so as to form an electrical path between an upper surface of the epitaxial layer and the at least one diffusion region; and

substantially filling the at least one trench with a filler material;

wherein the step of doping at least one or more sidewalls of the at least one trench is performed after the step of forming the at least one diffusion region.

2. (Original) The method of claim 1, wherein the step of forming the at least one diffusion region comprises the steps of:

implanting the bottom wall of the at least one trench with a second impurity of a known concentration level; and

driving in the second impurity so as to substantially distribute the second impurity between the bottom wall of the at least one trench and the substrate.

3. (Original) The method of claim 1, further comprising the steps of:

polishing the upper surface of the epitaxial layer so that the upper surface of the epitaxial layer is substantially planar; and

forming an insulating layer on at least a portion of the upper surface of the epitaxial layer.

4. (Original) The method of claim 3, wherein the upper surface of the insulating layer is at least a portion of the upper surface of the semiconductor wafer.

5. (Original) The method of claim 1, wherein the step of forming the at least one trench comprises:

forming an insulating layer on at least a portion of the upper surface of the epitaxial layer;

forming at least one opening in the insulating layer corresponding to the at least one trench; and

etching partially into the epitaxial layer.

6. (Original) The method of claim 1, wherein the at least one trench comprises a v-groove.

7. (Original) The method of claim 1, wherein the step of doping at least one or more sidewalls of the at least one trench with an impurity comprises:

cleaning the sidewalls of the at least one trench to substantially remove any organic material in the at least one trench;

predepositing the first impurity on at least one or more sidewalls of the at least one trench; and

driving in the first impurity.

8. (Original) The method of claim 7, wherein the first impurity comprises boron.

9. (Currently amended) The method of claim ~~6~~ 7, wherein the step of driving in the first impurity comprises heating the semiconductor wafer for a designated period of time.

10. (Original) The method of claim 9, wherein the step of heating the semiconductor wafer comprises heating the semiconductor wafer at a temperature in a range of about 900 degrees Celsius to about 1200 degrees Celsius for a duration of about one hour.

11. (Original) The method of claim 7, wherein the step of predepositing the first impurity on at least one or more sidewalls of the at least one trench comprises growing an impurity-rich oxide on at least one or more sidewalls of the at least one trench.

12. (Original) The method of claim 1, wherein the step of substantially filling the at least one trench comprises depositing a semiconductor material in the at least one trench so as to substantially fill the trench.

13. (Original) The method of claim 1, wherein the filler material comprises polysilicon material.

14. (Original) The method of claim 1, further comprising the step of forming at least one insulating layer on at least a portion of the upper surface of the epitaxial layer.

15. (Original) The method of claim 1, further comprising the step of:

forming an active device in the epitaxial layer proximate the upper surface of the epitaxial layer, the active device being in electrical connection with a first end of the at least one trench, a second end of the at least one trench being electrically connected to the substrate.

16. (Original) The method of claim 15, wherein the active device comprises a metal-oxide-semiconductor device.

17. (Original) The method of claim 1, further comprising the steps of:

forming an insulating layer on at least a portion of the upper surface of the epitaxial layer;

forming a gate on at least a portion of the insulating layer;

forming source and drain regions of a second conductivity type in the epitaxial layer proximate the upper surface of the epitaxial layer, the source and drain regions being spaced laterally from one another, the gate being formed at least partially between the source and drain regions, the source region being electrically connected to a first end of the at least one trench and a second end of the at least one trench being electrically connected to the substrate.

18. (Original) The method of claim 1, wherein the step of forming at least one trench comprises forming a plurality of trenches in the upper surface of the semiconductor wafer and partially into the epitaxial layer, at least two of the trenches being spaced about five microns apart relative to one another.

19. (Original) The method of claim 1, wherein the at least one trench is formed less than about 1.2 microns in width.

20 - 26 (Canceled)